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Methods Of Forming A Base Plate For A Field Emission Display (FED) Device, Methods Of Forming A Field Emission Display (FED) Device, Base Plates For Field Emission Display (FED) Devices, And Field Emission Display (FED) Devices

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METHODS OF FORMING A BASE PLATE FOR A FIELD EMISSION DISPLAY (FED) DEVICE, METHODS OF FORMING A FIELD EMISSION DISPLAY (FED) DEVICE, BASE PLATES FOR FIELD EMISSION DISPLAY (FED) DEVICES, AND FIELD EMISSION DISPLAY (FED) DEVICES

PATENT RIGHTS STATEMENT

This invention was made with Government support under Contract No. DABT63-97-C-0001 awarded by Advanced Research Projects Agency (ARPA). The Government has certain rights in this invention.

TECHNICAL FIELD

This invention relates to methods of forming a base plate for a field emission display (FED) device, to methods of forming a field emission display (FED) device, to base plates for field emission display (FED) devices, and to field emission display (FED) devices.

BACKGROUND OF THE INVENTION

Flat-panel displays are widely used to visually display information where the physical thickness and bulk of a conventional cathode ray tube is unacceptable or impractical. Portable electronic devices and systems have benefitted from the use of flat-panel displays, which require less space and result in a lighter, more compact display system than provided by conventional cathode ray tube technology.

The invention described below is concerned primarily with field emission flat-panel displays or FEDs. In a field emission flat-panel display, an electron emitting cathode plate is separated from a display

face or face plate at a relatively small, uniform distance. The intervening space between these elements is evacuated. Field emission displays have the outward appearance of a CRT except that they are very thin. While being simple, they are also capable of very high resolutions. In some cases they can be assembled by use of technology already used in integrated circuit production.

Field emission flat-panel displays utilize field emission devices, in groups or individually, to emit electrons that energize a cathodoluminescent material deposited on a surface of a viewing screen or display face plate. The emitted electrons originate from an emitter or cathode electrode at a region of geometric discontinuity having a sharp edge or tip. Electron emission is induced by application of potentials of appropriate polarization and magnitude to the various electrodes of the field emission device display, which are typically arranged in a two-dimensional matrix array.

Field emission display devices differ operationally from cathode ray tube displays in that information is not impressed onto the viewing screen by means of a scanned electron beam, but rather by selectively controlling the electron emission from individual emitters or select groups of emitters in an array. This is commonly known as "pixel addressing." Various displays are described in U.S. Patent Nos. 5,655,940, 5,661,531, 5,754,149, 5,563,470, and 5,598,057 the disclosures of which are incorporated by reference herein.

Fig. 1 illustrates a cross-sectional view of an exemplary field emission display (FED) device 10. Device 10 comprises a face plate 12, a base plate 14, and spacers 16 extending between base plate 14 and face plate 12 to maintain face plate 12 in spaced relation relative to base plate 14. Face plate 12, base plate 14 and spacers 16 can comprise, for example, glass. Phosphor regions 18, 20, and 22 are associated with face plate 12, and separated from face plate 12 by a transparent conductive layer 24. Transparent conductive layer 24 can comprise, for example, indium tin oxide or tin oxide. Phosphor regions 18, 20, and 22 comprise phosphor-containing masses. Each of phosphor regions 18, 20, and 22 can comprise a different color phosphor. Typically, the phosphor regions comprise either red, green or blue phosphor. A black matrix material 26 is provided to separate phosphor regions 18, 20, and 22 from one another.

Base plate 14 has emitter regions 28, 30 and 32 associated therewith. The emitter regions comprise emitters or field emitter tips 34 which are located within radially symmetrical apertures 36 (only some of which are labeled) formed through a conductive gate layer 38 and a lower insulating layer 40. Emitters 34 are typically about 1 micron high, and are separated from base plate 14 by a conductive layer 42. Emitters 34 and apertures 36 are connected with circuitry (not shown) enabling column and row addressing of the emitters 34 and apertures 36, respectively.

A voltage source 44 is provided to apply a voltage differential between emitters 34 and surrounding gate apertures 36. Application of such voltage differential causes electron streams 46, 48, and 50 to be emitted toward phosphor regions 18, 20, and 22 respectively. Conductive layer 24 is charged to a potential higher than that applied to gate layer 38, and thus functions as an anode toward which the emitted electrons accelerate. Once the emitted electrons contact phosphor dots associated with regions 18, 20, and 22 light is emitted. As discussed above, the emitters 34 are typically matrix addressable via circuitry. Emitters 34 can thus be selectively activated to display a desired image on the phosphor-coated screen of face plate 12.

The face plate typically has red, green and blue phosphor regions with black matrix areas 26 surrounding the phosphor regions. The three phosphor colors (red, green, and blue) can be utilized to generate a wide array of screen colors by simultaneously stimulating one or more of the red, green and blue regions.

As displays such as the one described above continue to grow in size and complexity, challenges are posed with respect to their design. For example, small-sized FED devices typically have a high resolution. As such displays grow in size, such resolution is desired to be maintained or even improved, yet challenges exist because of the increased dimensions. One such challenge is manifest in the video rate requirement in larger-area displays. The video rate requirement is typically determined by the RC time constant of the device. Typically,

address lines (e.g., row and column address lines) extend the entire length or width dimension respectively, of the addressable matrix of field emitters. Larger displays call for larger matrices. With larger matrices, such address lines can extend for greater lengths. Such greater lengths, accordingly, carry with them higher RC time constants which adversely impact the video rate requirement. Other challenges in the design of the larger-area display will be apparent to those of skill in the art.

One solution which has been proposed in the past (see, e.g. U.S. Patent No. 5,655,940) is to provide separate emitter plates which are subsequently mounted on a substrate to provide a larger-area display. This approach, however, can be inadequate and can result in much more processing complexity than is desirable. Specifically, multiple emitter plates must be separately formed and positioned relative to one another on a substrate. The plates must be precisely positioned to avoid anomalies in the subsequently rendered image. Needless to say, this can be a time-consuming process and results in more processing complexity than is desirable.

Accordingly, this invention arose out of concerns associated with providing improved field emission display (FED) devices and methods of forming such devices. This invention also arose out of concerns associated with providing larger-area FED displays with little or no additional processing complexity.

SUMMARY OF THE INVENTION

Methods of forming base plates for field emission display (FED) devices, methods of forming field emission display (FED) devices, and resultant FED base plate and device constructions are described. In one embodiment, a substrate is provided and is configurable into a base plate for a field emission display. A plurality of discrete, segmented regions of field emitter tips are formed by at least removing portions of the substrate. The regions are electrically isolated into separately-addressable regions. In another embodiment, a plurality of field emitters are formed from material of the substrate and arranged into more than one demarcated, independently-addressable region of emitters. Address circuitry is provided and is operably coupled with the field emitters and configured to independently address individual regions of the emitters. In yet another embodiment, a monolithic addressable matrix of rows and columns of field emitters is provided and has a perimetral edge defining length and width dimensions of the matrix. The matrix is partitioned into a plurality of discretely-addressable sub-matrices of field emitters. Row and column address lines are provided and are operably coupled with the matrix and collectively configured to address the field emitters. At least one of the row or column address lines has a length within the matrix which is sufficient to address less than all of the field emitters which lie in the direction along which the address line extends within the matrix.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a side sectional view of a portion of an exemplary field emission display (FED) device which can be constructed in accordance with one or more embodiments of the present invention.

Fig. 2 is a somewhat schematic view of a FED base plate and address circuitry in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 2, and in accordance with one embodiment of the present invention, a substrate 52 is provided and is configurable into a base plate for a field emission display (FED). In the illustrated example, substrate 52 corresponds to base plate 14 of Fig. 1. A plurality of discrete, segmented regions of field emitter tips (such as field emitters or emitter tips 34 in Fig. 1) are formed by removing portions of the substrate, preferably through known etching techniques. Exemplary discrete, segmented regions are shown in Fig. 2 at 54, 56, 58 and 60. In a preferred embodiment, regions 54-60 are electrically isolated from one another into separately-addressable regions of field

emitter tips. In the illustrated and preferred embodiment, four regions are formed. It is possible, however, for different numbers of regions to be formed. For example, in one embodiment at least two regions are formed. In another embodiment, at least three regions are formed. More than four regions can be formed, e.g. six, eight, ten, twelve and the like. Additionally, other than even numbers of regions can be formed as, for example, three, five, seven and the like.

In another embodiment, formation of the discrete, segmented regions comprises etching the substrate into the formed regions. In a preferred embodiment, the base plate, as formed, comprises a monolithic base plate of field emitter tips. By providing a monolithic base plate with the plurality of discrete, segmented regions, advantages are achieved over prior devices. For example, the monolithic nature of various of the preferred embodiments can reduce processing complexities by requiring processing of only one work piece, e.g. substrate 52, in order to form the base plate. In addition, resolution of the ultimately-formed device can be improved because of the uniformity of the material from which the base plate is formed. Specifically, by forming the illustrated discrete, segmented, and electrically-isolated regions from a common substrate, uniformity in the ultimately provided image can be enhanced.

In another embodiment, address circuitry is provided and operably coupled with substrate 52. Preferably, the address circuitry is configured to separately address individual regions of the field emitter tips. In the illustrated example of Fig. 2, the address circuitry comprises row drivers

and column drivers. Each individual region has its own row driver and column driver. Individual row and column drivers are arranged in groupings designated at 62, 64, 66, and 68 for each individual region. Specifically, the row and column drivers in grouping 62 are provided for addressing region 54; the row and column driver in grouping 64 are provided for addressing region 56; the row and column driver in grouping 66 are provided for addressing region 60; and the row and column driver in grouping 68 are provided for addressing region 58. The individual row and column drivers are connected with individual row and column lines which extend though the individual regions. The row and column lines are typically formed by depositing a conductive material, and then using a photomask to define the conductive line patterns which are subsequently etched from the conductive material. Here, in order to form the separately-addressable regions, the photomask is modified such that the subsequently-etched row and column lines do not extend across the entirety of the addressable matrix, but rather only partially across the matrix in regions corresponding to those illustrated in Fig. 2.

In one embodiment, a face plate, such as face plate 12 in Fig. 1, is provided and supports areas of luminescent material. Exemplary luminescent material areas are shown at 18, 20, and 22. Face plate 12 is preferably mounted in operable proximity with substrate 52 to provide a field emission display (FED) device.

In another embodiment, a plurality of field emitters, such as emitters 34 in Fig. 1, are formed from material of the substrate, which, in this example, corresponds to substrate 14. The emitters are arranged into more than one demarcated, independently-addressable region of emitters. Exemplary demarcated, independently-addressable regions are shown in Fig. 2 at 54, 56, 58, and 60. Demarcation of the individual regions occurs along lines 70, 72. Address circuitry, such as that described above, is preferably provided and operably coupled with the field emitters and configured to independently address the individual regions of emitters. In one embodiment, the emitters are arranged into more than two demarcated, independently-addressable regions of emitters. In another embodiment, the emitters are arranged into more than three demarcated, independently-addressable regions of emitters. In a preferred embodiment, the emitters are arranged into four demarcated, independently-addressable regions of emitters. In the illustrated example, demarcation of the individual regions of emitters takes place by forming address lines, e.g. row and column lines which are effectively contained within the individual respective regions, and which do not extend into any other individual region. Such can be accomplished by using a photomask which defines the individual address lines within each region.

In another embodiment, the arrangement of emitters defines a plurality of rows and columns within each region. In this example, portions of exemplary rows and columns are schematically shown within each of regions 54-60 as cross-hatched areas. In this example, provision

of the address circuitry comprises providing at least two separate row drivers for addressing rows in different regions of the emitters. For example, in the illustrated example, region 54 has its own row driver which comprises part of grouping 62. Similarly, region 56 has its own row driver which comprises part of grouping 64. In another embodiment, provision of the address circuitry comprises providing at least two separate column drivers for addressing columns in different regions of the emitters. For example, region 54 has its own column driver which comprises part of grouping 62. Likewise, region 56 has its own column driver which comprises part of grouping 64. In a preferred embodiment, provision of the address circuitry comprises providing at least two separate row drivers and at least two separate column drivers for addressing the rows and columns in different respective regions of the emitters. In the illustrated example, four exemplary regions, i.e. regions 54-60, are provided. Each region has its own row driver and column driver.

In another embodiment, a monolithic addressable matrix of rows and columns of field emitters is provided. In this example, the monolithic addressable matrix corresponds to substrate 52 of Fig. 2. The matrix has a perimetral edge 74 which defines length and width dimensions L, W respectively, of the matrix. The matrix is partitioned into a plurality of discretely-addressable sub-matrices of field emitters. Exemplary sub-matrices are shown at 54, 56, 58, and 60. Row and column address lines are provided and are operably coupled with the

matrix. The row and column address lines (shown schematically as cross-hatched areas in each of the regions) are collectively configured to address the field emitters in each region. At least one of the row or column address lines has a length within the matrix which is sufficient to address less than all of the field emitters which lie in the direction along which the address line extends within the matrix. As an illustrative example, consider row address line R_X in sub-matrix 58. Row address line R_X extends in a direction A within the matrix defined by perimetral edge 74. Row address line R_X has a length within the matrix defined by the perimetral edge which is sufficient to address less than all of the field emitters which lie in the direction along which line R_X extends within the matrix. Specifically, in this example, row address line R_X can address field emitters only within sub-matrix 58, and not within sub-matrix 60 which lie in a common direction with direction A. The same can be said for the other row address lines and their respective sub-matrices, as well as the other column address lines and their sub-matrices.

In one embodiment, the length of the one row or column address line within the matrix is less than a length (L) or width (W) dimension of the matrix. In another embodiment, the length of the one row or column address line within the matrix is less than a length or width dimension of one of the sub-matrices.

In one embodiment, the partitioning of the matrix comprises partitioning the matrix into more than two sub-matrices. In another

embodiment, the matrix is partitioned into more than three sub-matrices. In a preferred embodiment, the matrix is partitioned into four sub-matrices.

In yet another embodiment, a field emission display (FED) face plate comprises a monolithic substrate configured into a base plate for a field emission display (FED). The base plate comprises a plurality of regions of field emitter tips which comprise material of the substrate. Individual regions of the plurality of regions are discrete and electrically isolated from one another and are configured to be separately addressed. An exemplary base plate is shown in Fig. 2 at 52. In one embodiment, the substrate comprises at least two regions of field emitter tips. In another embodiment, the substrate comprises at least three regions of field emitter tips. In a preferred embodiment, the substrate comprises at least four regions of field emitter tips.

Various advantages can be achieved by the embodiments described above. Improvements can be achieved in the refresh rates of the ultimately-formed FED devices which are faster than those of identical displays with non-partitioned base plates. This is because the RC time constant scales linearly with the length of the address lines, i.e. row and column address lines. In addition, larger displays can be constructed for applications where a large viewing area is desired, such as an engineering work-station or for presentations to larger groups of people in a conference room setting. Additionally, higher resolution can be achieved in larger displays which is comparable with the resolution in

smaller displays. Moreover, multiple images can be viewed and updated independently of other images.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.